Patent Claims

1. A method for generating multiplier coefficients for a (1:m) mixer, comprising the following steps:

(a) recursive calculating of a multiplier set (MS);

(b) selecting a multiplier group (MG), consisting of a number of multipliers, from the calculated multiplier set (MS) in dependence on a predetermined signal/noise ratio (SNR_{NOM}) of the mixer

(c) writing multiplier coefficients (MC) into a memory of the mixer in accordance with the selected multiplier group (MG).

2. The method as claimed in claim 1, wherein the mixer is a 1:10 mixer,
in which, during the recursive calculation, after initialization of a first multiplier V_0 of the multiplier set (MS) to zero ($V_0 = 0$) and
of a second multiplier V_1 of the multiplier set (MS) to one ($V_1 = 1$),
the further multipliers of the multiplier set (MS) are calculated in accordance with the following recursion rule:
$V_{i+2} = V_i + V_{i+1}$ for all $i = 0, 1, 2 \ldots i_{max}$

3. The method as claimed in claim 2,
wherein
a multiplier group (MG) consisting of two multipliers (V_i, V_{i+1}) is selected from the multiplier set (MS), the run index i of which produces a signal/noise ratio

$$(SNR) = 20\log\left[\frac{1+\sqrt{5}}{2}\right]^2 \cdot \left(i + \frac{1}{2}\right)$$

which is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

4. The method as claimed in claim 3, wherein the following multiplier coefficients (MC) are written into the memory:

$$MC = (0,\ V_i,\ V_{i+1},\ V_{i+1},\ V_i,\ 0,\ -V_i,\ -V_{i+1},\ -V_{i+1}\ -V_i).$$

5. The method as claimed in claim 2, wherein a multiplier group (MG) consisting of three multipliers (V_i, V_{i+1}, V_{i+2}) is selected from the multiplier set (MS), the run index i of which produces a signal/noise ratio

$$(SNR) = 20\log\left[\frac{1+\sqrt{5}}{2}\right]^2 \cdot (i+1)$$

which is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

6. The method as claimed in claim 5, wherein the following multiplier coefficients (MC) are written into the memory of the mixer:

$$MC = (V_i,\ V_{i+2},\ 2*V_{i+2},\ V_{i+2},\ V_i,\ -V_i,\ -V_{i+2},\ -2*V_{i+2},\ -V_{1+2}\ -V_i)$$

7. The method as claimed in claim 1, wherein the mixer is a 1:8 mixer, in which, during the recursive calculation, after initialization of a first multiplier V_0 of the multiplier set to zero ($V_0 = 0$) and of a second multiplier V_1 of the multiplier set (MS) to one ($V_1 = 1$), the further multipliers of the multiplier set

(MS) are calculated in accordance with the following recursion rule:

$V_{i+2} = V_i + V_{i+1}$

$V_{i+3} = V_i + V_{i+2}$

for all even-numbered $i = 0, 2, 4 \ldots i_{max}$

8. The method as claimed in claim 7, in which a multiplier group (MG) consisting of two multipliers (V_i, V_{i+1}) is selected from the multiplier set (MS), the run index i of which produces a signal/noise ratio $SNR = 20 \log \left(1 + \sqrt{2}\right) * i$ which is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

9. The method as claimed in claim 1, wherein the following multiplier coefficients (MC) are written into the memory of the mixer:

$MC = (0, V_i, V_{i+1}, Vi, 0, -V_i, -V_{i+1}, -V_i)$

10. The method as claimed in claim 7, in which a multiplier group (MG) consisting of two multipliers (V_i, V_{i+1}) is selected from the multiplier set (MS), the run index i of which produces a signal/noise ratio $SNR = 20 \log \left[1 + \sqrt{2}\right] (i+1)$ which is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

11. The method as claimed in claim 10, in which the following multiplier coefficients (MC) are written into the memory of the mixer:

$MC = (V_i, V_{i+2}, V_{i+2}, V_i, -V_i, -V_{i+2}, -V_i)$

12. The method as claimed in claim 1,

wherein
the mixer is a 1:12 mixer,
in which, during the recursive calculation, after initialization of a first multiplier V_0 of the multiplier set (MS) to one ($V_0 = 1$) and of a second multiplier V_1 of the multiplier set (MS) to one ($V_1 = 1$), the further multipliers of the multiplier set (MS) are calculated in accordance with the following recursion rule:

$$V_{i+2} = V_i + 2*V_{i+1}$$
$$V_{i+3} = V_i + V_{i+1}$$
$$V_{i+4} = V_i + 2*V_{i+2}$$
$$V_{i+5} = V_i + 3*V_{i+1}$$

for all $i = 0, 4, 8 \ldots i_{max}$

13. The method as claimed in claim 12,
in which
a multiplier group (MG) consisting of two multipliers (V_i, V_{i+2}) is selected from the multiplier set (MS), the run index i of which produces a signal/noise ratio $SNR = 20\log\left[\sqrt{2+\sqrt{3}}\right] \cdot (i+2)$ which is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

14. The method as claimed in claim 13,
in which
the following multiplier coefficients (MC) are written into the memory of the mixer:

$$MC = (0,\ V_i,\ V_{i+2},\ 2*V_i,\ V_{i+2},\ V_i,\ 0,\ -V_i,\ -V_{i+2},\ -2*V_i,\ -2*V_{i+2},\ -V_i).$$

15. The method as claimed in claim 12,
in which
a multiplier group consisting of two multipliers (V_{i+3} V_{i+4}) is selected from the multiplier set (MS),

the run index i of which produces a signal/noise ratio $SNR = 20\log\left[\sqrt{2+\sqrt{3}}\right] \cdot (i+5)$ which is higher than the predetermined signal/noise ratio SNR_{NOM} of the mixer.

16. The method as claimed in claim 15, in which the following multiplier coefficients (MC) are written into the memory of the mixer:

$MC = (V_i,\ V_{i+3},\ V_{i+4},\ V_{i+4},\ V_{i+3},\ V_i,\ -V_i,\ -V_{i+3},\ -V_{i+4},\ -V_{i+4},\ -V_{i+3},\ -V_i)$

17. The method as claimed in one of the preceding claims, wherein the multiplier of the multiplier groups (MG) are resolved into Horner coefficients.

18. A mixer for mixing a digital input signal with a sampled sinusoidal signal, comprising:

(a) a multiplier unit for multiplying the digital input signal by multiplier coefficients (MC);

(b) and a coefficient memory for storing multiplier coefficients (MC) which can be applied to the multiplier unit by means of an address generator,

(c) and comprising a connectable coefficient generator for generating the multiplier coefficients (MC) by recursive calculation of a multiplier set (MS) from which a multiplier group (MG) consisting of a number of multipliers is selected in dependence on a predetermined signal/noise ratio SNR_{NOM} of the mixer and corresponding multipliers (MC) are written into the coefficient memory.

19. The mixer for mixing a digital input signal with a sampled sinusoidal signal, comprising:

(a) a calculating circuit for calculating multipliers (MC) of a multiplier group (MG), which exhibits a number of dividing circuits for dividing the digital input signal applied to an input of the mixer, and a number of switchable adders/subtractors,

- the dividing factors of the dividing circuits being Horner coefficients of the resolved multipliers (MC) of the multiplier group (MG),

- the adders/subtractors being controlled in dependence on a first control bit (SUB/ADD) read out of a memory;

(b) a demultiplexer for switching through a zero value or the multiplier (MC) calculated by the calculating circuit in dependence on a second control bit (zero) read out of the memory; and comprising

(c) a sign circuit for outputting the positive or negative value switched through by the demultiplexer to an output of the mixer in dependence on a third control bit (SIGN) read out of the memory.

20. The mixer as claimed in claim 19, wherein the dividing circuits are shift registers.

21. The mixer as claimed in claim 19, wherein an address generator is provided for reading out the control bits from the memory.

22. The mixer as claimed in claim 21, wherein the memory is a read-only memory (ROM).

23. The mixer as claimed in claim 21, wherein the memory is programmable.